Tzen-Chuen Ng

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Education

Carnegie Mellon University — Pittsburgh, PA
Bachelor of Science in Electrical and Computer Engineering, QPA 3.51 — *May 2025*
Bachelor of Science in Engineering and Public Policy — *May 2025*

Projects

Custom RISC-V CPU | *SystemVerilog* — Apr. 2025

- Built a 7 stage multi-cycle pipelined CPU, reaching 2.5x speedup from single-cycle
- Added features such as branch prediction, data forwarding, and caching reducing pipeline stalls by 75%
- Tracked execution statistics with a performance monitoring system, allowing further insight for opimization
- Simulated design with Synopsis VCS and analyzed area, power, and critical path, resulting in a 340 MHz clock

Dashcam ALPR | *Python* — Apr. 2025

- Built a dashcam with automatic license plate recognition to search for vehicles matching active Amber Alerts
- Fine tuned OCR and object detection models (PaddleOCR, Yolov11), achieving a 98.7% precison and 79.1% recall at 15 meters on a Raspberry Pi 4 and Arducam IMX519
- Worked with Supabase edge functions and Amazon Rekognition for validation edge compute matches

USB Serial Interface Engine | *SystemVerilog* — Apr. 2024

- Implemented NZRI encoding/decoding, bit stuffing and a complex protocol handler FSM
- Wrote CRC-16 error detection with recovery mechanisms for up to 7 data packet transactions
- Verified components and entire design with modular tests (corrupted packets, timeout, etc) with SV assertions

Experience

Teaching Assistant (Computer Systems) — Summer 2024
Carnegie Mellon University — *Pittsburgh, PA*

- Led two weekly 5-student groups by hosting discussions on material, 1-on-1 time for specific questions, planning course content, and holding general office hours
- Worked with professor to incorporate feedback to enhance material and improve student learning

Full Stack Intern — Summer 2023
GBG Plc — *Palo Alto, CA*

- Coded in Typescript using React to maintain and update component testcases
- Created monitoring tools for tracking program query times, latency, and server load
- Familiarized myself with large, mature codebases and learned the principles behind the creation and development of production-ready code

Test Automation Intern — Summer 2022
Aviva Links — *San Jose, CA*

- Coded SCPI/Python to control GPIB-based test and measurement equipment
- Helped design/validation/verification teams bring up new silicon compliant to Automotive Serdes Alliance connectivity standard with Python scripts for automated testing
- Enabled feedback mechanisms in testing scripts such as logging and email monitoring

Technical Skills

Programming: Python, C, C++, Go, Java, MATLAB, Bash
Hardware Design: SystemVerilog (RTL, SVA), Assembly (x86, RISC-V), FPGA prototyping, CPU Microarchitecture
Tools: Synopsis VCS, Synopsis Design Compiler, Quartus, Cadence Virtuoso
Languages: English (Native), Chinese (Fluent)